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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,318	HENSBERGEN ET AL.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *3,13,18,23 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03 December 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 03 December 2003 was filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

Claims 3, 13, 18, 23 and 28 are objected to because of the following informalities:

- Claim 18 recites the limitation "said system energy usage" in lines 3-4 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is also recited that claim 18 is dependent on claim 11. Given the claim pattern of claims 1-10, the Examiner asserts that the intention of the Applicant was to have claim 18 dependent on 17. Please change "The processing system of Claim 11," on line 1 of claim 18 to "The processing system of Claim 17,"
- Claim 28 recites the limitation "said system energy usage" in lines 3-4 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is also recited that claim 28 is dependent on claim 21. Given the claim pattern of claims 1-10, the Examiner asserts that the intention of the Applicant was to have claim 28 dependent on 27. Please change "The processing system of Claim 21," on line 1 of claim 28 to "The processing system of Claim 27,"

- Claims 13 and 23 recite "during or more" on line 4 of both claims and claim 3 recites "during or more" on line 3. The Examiner asserts the intention of the Applicant was to have the claims read *during one or more*. Please change claims 3, 13 and 23 to read "during one or more" respectively.

Appropriate correction is required. The following Office Action will be examined based upon the correction requests stated above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maitra (U.S. Patent No. 5,623,647) (hereinafter referred to as Maitra) in view of Tobias (U.S. Patent No. 6,996,441 B1) (hereinafter referred to as Tobias).

As to claim 1, Maitra discloses a method of managing energy in a processing system, comprising: receiving an indication of a need to reduce a energy usage level in said processing system at a scheduler (Maitra discloses a scheduler [clock scheduling unit 120] that is part of the operating system which retrieves information needed to determine if the CPU clock needs to be throttled which, as is known in the art, reducing the energy usage; column 4, lines 56-64 and column 8, line 45 thru column 9, line 4); determining whether or not a next process to be scheduled has an associated level of energy usage ("performance level") (Maitra discloses the

clock scheduling unit [120] determining whether the microprocessor is operating at a performance level appropriate for the applications running; column 4, line 56 thru column 5, line 3); and, selectively scheduling (via the task scheduling unit 110) an execution slice ("time quantum" or "time slice") for said next process in response to determining that said associated level of energy usage (Maitra discloses the task scheduling unit [110] assigning time slices associated with the applications running on the processor as a result of the performance level determination mentioned above; column 4, lines 25-37 and column 4, lines 56-67).

Maitra does not disclose the energy usage determination using a threshold or if said energy usage level is greater than said threshold.

Tobias teaches a fan control system and method to control the speed of a fan to help dissipate heat wherein said fan control system might be a part of a multi-featured power control daemon (170) (column 2, lines 26-42 and column 4, lines 22-24 and column 4, lines 41-43). The said power control daemon (170) above further includes adjusting the CPU (processor 110) performance dependent on information gathered and statistics calculated from the operating system (OS) of the system and the control daemon (170) (column 4, lines 50-63). Tobias further explains that the OS of the system allocates time slices for applications and if the time slices are not being utilized by the CPU then the performance of the CPU can be "ratcheted down" which therefore would be inclusive of ratcheting the processor up (column 4, lines 63 thru column 5, line 2). Tobias further explains various other performance characteristics that can be used to determine the utilization of the processor to include, voltage level and frequency (column 5, lines 10-28). The performance predictions based upon utilization require the use of a threshold to determine if the clock fan will be increased or decreased (which would be inclusive of increasing

or decreasing CPU performance as well as mentioned hereinabove) (column 2, lines 26-42 and column 6, lines 19-46). Tobias has the added advantage of including fan control to help manage heat dissipation in the system in addition to the processor utilization increasing and decreasing (column 2, lines 15-25).

It would have been obvious to one of ordinary skill of the art having the teachings of Maitra and Tobias at the time the invention was made, to modify the OS scheduler of Maitra to include a control daemon to include power management control techniques to include the use of thresholds of the power usage dependent on various performance characteristics as taught by Tobias such that OS scheduler of Maitra has the capability of determining whether future processes exceed an energy level threshold and scheduling extra execution slices if said threshold is not exceeded. One of ordinary skill in the art would be motivated to make this combination of adjusting performance of a processor dependent on performance characteristics and thresholds in view of the teachings of Tobias, as doing so would give the added advantage of including fan control to help manage heat dissipation in the system in addition to the processor utilization increasing and decreasing (column 2, lines 15-25).

As to claim 2, Maitra discloses the method further comprising: reading values ("accessing" information which necessitates reading) of a plurality of performance counters (Maitra discloses the clock scheduling unit collecting information from a task scheduler unit which prioritizes applications dependent on the amount of time used by the process which, as is known the art, necessitates performance counters to calculate usage; column 8, lines 55-61) during one or more previous execution slices (time quantum) of said next process (column 2, lines 49-67); and estimating ("prioritizing") said associated level of energy usage ("determines

the amount of CPU time each application receives") in conformity with said values of said plurality of performance counters (column 8, line 45 thru column 9, line 4).

As to claim 3, Maitra discloses the method further comprising: measuring ("retrieves information") actual energy usage of said processing system ("computing requirement") during one or more previous execution slices of said next process ("next quantum") (column 8, lines 47-64); and estimating ("determining") said associated level of energy usage in conformity with said measured energy usage (column 8, lines 47-64).

As to claim 4, Maitra discloses the method further comprising: second determining ("determines the applications run" via switch detection unit [210] found in clock scheduling unit [120 or 200]) a resource usage of said next process (column 5, lines 10-13 and column 5, lines 31-40 and column 5, line 54 thru column 6, line 14); and estimating ("determines the computing requirement" via application characterization unit [220]) said associated level of energy usage in conformity with said resource usage (column 6, lines 1-14).

As to claim 5, Maitra discloses the method further comprising receiving from an application owning said next process an indication of said resource usage (column 6, lines 4-14), and wherein said determining determines said resource usage ("computing requirements") in conformity with said received indication (column 6, lines 1-14).

As to claim 6, Tobias teaches the method wherein said second determining is performed by said operating system by observing prior allocation of resources to said next process (column 4, lines 52-67 and column 2, lines 15-25).

As to claim 7, Tobias teaches the method further comprising: issuing a pragmatic warning fault ("bit being sent") indicating that a system energy usage above a system energy

threshold (column 1, lines 39-42); and receiving ("predicting" heat based on CPU performance which necessitates receiving) said pragmatic warning fault ("performance indicators") at an application associated with said next process, and in response to said receiving, reducing a resource usage within said application, whereby a energy usage of said next process is reduced (column 2, lines 26-42).

As to claim 8, Tobias teaches the method further comprising: issuing ("signal indicative of the temperature of system [100] is received and processed") a critical pragmatic fault indicating ("failsafe signal") that said system energy usage has not been reduced below said system energy threshold (column 4, lines 25-36); and receiving ("control transitions" which necessitates receiving) said critical pragmatic fault at said scheduler (control daemon), and wherein said selectively scheduling is performed in response to said receipt of said critical pragmatic fault by said scheduler (Tobias discloses a flowchart [figure 2] which reveals the steps needed in decision making of altering the fan speed wherein said flow returns to step 210 repetitively wherein flow could flow to normal alteration to step 240 or to a critical response to 230; column 4, lines 25-36).

As to claim 9, Maitra discloses the method wherein said selectively scheduling inserts idle slices ("device may be turned off" or "asserts and de-asserts an internal clock divider mechanism in the processor") into an execution queue ("list of applications that need to be run"), whereby said energy usage level is reduced (Maitra discloses time slices places into a list of applications to be run wherein said clock to functional units within the processor can be de-asserted if not needed which therefore necessitates inserting idle slices [periods of inactivity]; column 1, line 63 thru column 2, line 1 and column 4, lines 35-55 and column 5, lines 33-40).

As to claim 10, Maitra discloses the method wherein said selectively scheduling schedules a second process having a lower level of energy usage than said next process in preference over said next process (Maitra discloses a priority list of applications being implemented wherein applications are run dependent on the size of the quantum such that internally defined priorities can decide which applications run next dependent on their high or low energy usage; column 4, lines 44-55).

As to claim 11, Maitra discloses a processing system, comprising: a processor (410); a memory (420) coupled to said processor (column 7, lines 66-67) for storing program instructions and data values (column 7, lines 63-65), and wherein said program instructions comprise an operating system scheduler (Maitra discloses a task scheduling unit [110] that is part of the operating system; column 8, lines 58-60) that includes program instructions (Maitra discloses the operating system and other programs stored in memory [420]; column 8, 2-7) for: receiving an indication of a need to reduce a energy usage level in said processing system at a scheduler (Maitra discloses a scheduler [clock scheduling unit 120] that is part of the operating system which retrieves information needed to determine if the CPU clock needs to be throttled which, as is known in the art, reducing the energy usage; column 4, lines 56-64 and column 8, line 45 thru column 9, line 4); determining whether or not a next process to be scheduled has an associated level of energy usage ("performance level") (Maitra discloses the clock scheduling unit [120] determining whether the microprocessor is operating at a performance level appropriate for the applications running; column 4, line 56 thru column 5, line 3); and, selectively scheduling (via the task scheduling unit 110) an execution slice ("time quantum" or "time slice") for said next process in response to determining that said associated level of energy usage (Maitra discloses

the task scheduling unit [110] assigning time slices associated with the applications running on the processor as a result of the performance level determination mentioned above; column 4, lines 25-37 and column 4, lines 56-67).

Maitra does not disclose the energy usage determination using a threshold or if said energy usage level is greater than said threshold.

Tobias teaches a fan control system and method to control the speed of a fan to help dissipate heat wherein said fan control system might be a part of a multi-featured power control daemon (170) (column 2, lines 26-42 and column 4, lines 22-24 and column 4, lines 41-43). The said power control daemon (170) above further includes adjusting the CPU (processor 110) performance dependent on information gathered and statistics calculated from the operating system (OS) of the system and the control daemon (170) (column 4, lines 50-63). Tobias further explains that the OS of the system allocates time slices for applications and if the time slices are not being utilized by the CPU then the performance of the CPU can be "ratcheted down" which therefore would be inclusive of ratcheting the processor up (column 4, lines 63 thru column 5, line 2). Tobias further explains various other performance characteristics that can be used to determine the utilization of the processor to include, voltage level and frequency (column 5, lines 10-28). The performance predictions based upon utilization require the use of a threshold to determine if the clock fan will be increased or decreased (which would be inclusive of increasing or decreasing CPU performance as well as mentioned hereinabove) (column 2, lines 26-42 and column 6, lines 19-46). Tobias has the added advantage of including fan control to help manage heat dissipation in the system in addition to the processor utilization increasing and decreasing (column 2, lines 15-25).

It would have been obvious to one of ordinary skill of the art having the teachings of Maitra and Tobias at the time the invention was made, to modify the OS scheduler of Maitra to include a control daemon to include power management control techniques to include the use of thresholds of the power usage dependent on various performance characteristics as taught by Tobias such that OS scheduler of Maitra has the capability of determining whether future processes exceed an energy level threshold and scheduling extra execution slices if said threshold is not exceeded. One of ordinary skill in the art would be motivated to make this combination of adjusting performance of a processor dependent on performance characteristics and thresholds in view of the teachings of Tobias, as doing so would give the added advantage of including fan control to help manage heat dissipation in the system in addition to the processor utilization increasing and decreasing (column 2, lines 15-25).

As to claim 12, Maitra discloses the processing system wherein said program instructions further comprise program instructions for: reading values ("accessing" information which necessitates reading) of a plurality of performance counters (Maitra discloses the clock scheduling unit collecting information from a task scheduler unit which prioritizes applications dependent on the amount of time used by the process which, as is known the art, necessitates performance counters to calculate usage; column 8, lines 55-61) during one or more previous execution slices (time quantum) of said next process (column 2, lines 49-67); and estimating ("prioritizing") said associated level of energy usage ("determines the amount of CPU time each application receives") in conformity with said values of said plurality of performance counters (column 8, line 45 thru column 9, line 4).

As to claim 13, Maitra discloses the processing system wherein said program instructions further comprise program instructions for: measuring ("retrieves information") actual energy usage of said processing system ("computing requirement") during one or more previous execution slices of said next process ("next quantum") (column 8, lines 47-64); and estimating ("determining") said associated level of energy usage in conformity with said measured energy usage (column 8, lines 47-64).

As to claim 14, Maitra discloses the processing system wherein said program instructions further comprise program instructions for: second determining ("determines the applications run" via switch detection unit [210] found in clock scheduling unit [120 or 200]) a resource usage of said next process (column 5, lines 10-13 and column 5, lines 31-40 and column 5, line 54 thru column 6, line 14); and estimating ("determines the computing requirement" via application characterization unit [220]) said associated level of energy usage in conformity with said resource usage (column 6, lines 1-14).

As to claim 15, Maitra discloses the processing system wherein said program instructions further comprise program instructions (column 5, lines 63-67) for receiving from an application owning said next process an indication of said resource usage (column 6, lines 4-14), and wherein said determining determines said resource usage ("computing requirements") in conformity with said received indication (column 6, lines 1-14).

As to claim 16, Tobias teaches the processing system wherein said program instructions for second determining further comprise program instructions for observing prior allocation of resources to said next process (column 4, lines 52-67 and column 2, lines 15-25).

As to claim 17, Tobias teaches the processing system wherein said program instructions further comprise program instructions for: issuing a pragmatic warning fault ("bit being sent") indicating that a system energy usage above a system energy threshold (column 1, lines 39-42); and receiving ("predicting" heat based on CPU performance which necessitates receiving) said pragmatic warning fault ("performance indicators") at an application associated with said next process, and in response to said receiving, reducing a resource usage within said application, whereby a energy usage of said next process is reduced (column 2, lines 26-42).

As to claim 18, Tobias teaches the processing system wherein said program instructions further comprise program instructions for: issuing ("signal indicative of the temperature of system [100] is received and processed") a critical pragmatic fault indicating ("failsafe signal") that said system energy usage has not been reduced below said system energy threshold (column 4, lines 25-36); and receiving ("control transitions" which necessitates receiving) said critical pragmatic fault at said scheduler (control daemon), and wherein said selectively scheduling is performed in response to said receipt of said critical pragmatic fault by said scheduler (Tobias discloses a flowchart [figure 2] which reveals the steps needed in decision making of altering the fan speed wherein said flow returns to step 210 repetitively wherein flow could flow to normal alteration to step 240 or to a critical response to 230; column 4, lines 25-36).

As to claim 19, Maitra discloses the processing system wherein said program instructions for selectively scheduling insert idle slices ("device may be turned off" or "asserts and de-asserts an internal clock divider mechanism in the processor") into an execution queue ("list of applications that need to be run"), whereby said energy usage level is reduced (Maitra discloses time slices places into a list of applications to be run wherein said clock to functional units

within the processor can be de-asserted if not needed which therefore necessitates inserting idle slices [periods of inactivity]; column 1, line 63 thru column 2, line 1 and column 4, lines 35-55 and column 5, lines 33-40).

As to claim 20, Maitra discloses the processing system wherein said program instructions for selectively scheduling schedule a second process having a lower level of energy usage than said next process in preference over said next process (Maitra discloses a priority list of applications being implemented wherein applications are run dependent on the size of the quantum such that internally defined priorities can decide which applications run next dependent on their high or low energy usage; column 4, lines 44-55).

As to claim 21, Maitra discloses a computer program product comprising signal-bearing media encoding program instructions and data (column 3, line 58 thru column 2, line 21 and column 7, lines 63-65), wherein said program instructions comprise an operating system scheduler (Maitra discloses a task scheduling unit [110] that is part of the operating system; column 8, lines 58-60) that includes program instructions (Maitra discloses the operating system and other programs stored in memory [420]; column 8, 2-7) for: receiving an indication of a need to reduce a energy usage level in said processing system at a scheduler (Maitra discloses a scheduler [clock scheduling unit 120] that is part of the operating system which retrieves information needed to determine if the CPU clock needs to be throttled which, as is known in the art, reducing the energy usage; column 4, lines 56-64 and column 8, line 45 thru column 9, line 4); determining whether or not a next process to be scheduled has an associated level of energy usage ("performance level") (Maitra discloses the clock scheduling unit [120] determining whether the microprocessor is operating at a performance level appropriate for the applications

running; column 4, line 56 thru column 5, line 3); and, selectively scheduling (via the task scheduling unit 110) an execution slice ("time quantum" or "time slice") for said next process in response to determining that said associated level of energy usage (Maitra discloses the task scheduling unit [110] assigning time slices associated with the applications running on the processor as a result of the performance level determination mentioned above; column 4, lines 25-37 and column 4, lines 56-67).

Maitra does not disclose the energy usage determination using a threshold or if said energy usage level is greater than said threshold.

Tobias teaches a fan control system and method to control the speed of a fan to help dissipate heat wherein said fan control system might be a part of a multi-featured power control daemon (170) (column 2, lines 26-42 and column 4, lines 22-24 and column 4, lines 41-43). The said power control daemon (170) above further includes adjusting the CPU (processor 110) performance dependent on information gathered and statistics calculated from the operating system (OS) of the system and the control daemon (170) (column 4, lines 50-63). Tobias further explains that the OS of the system allocates time slices for applications and if the time slices are not being utilized by the CPU then the performance of the CPU can be "ratcheted down" which therefore would be inclusive of ratcheting the processor up (column 4, lines 63 thru column 5, line 2). Tobias further explains various other performance characteristics that can be used to determine the utilization of the processor to include, voltage level and frequency (column 5, lines 10-28). The performance predictions based upon utilization require the use of a threshold to determine if the clock fan will be increased or decreased (which would be inclusive of increasing or decreasing CPU performance as well as mentioned hereinabove) (column 2, lines 26-42 and

column 6, lines 19-46). Tobias has the added advantage of including fan control to help manage heat dissipation in the system in addition to the processor utilization increasing and decreasing (column 2, lines 15-25).

It would have been obvious to one of ordinary skill of the art having the teachings of Maitra and Tobias at the time the invention was made, to modify the OS scheduler of Maitra to include a control daemon to include power management control techniques to include the use of thresholds of the power usage dependent on various performance characteristics as taught by Tobias such that OS scheduler of Maitra has the capability of determining whether future processes exceed an energy level threshold and scheduling extra execution slices if said threshold is not exceeded. One of ordinary skill in the art would be motivated to make this combination of adjusting performance of a processor dependent on performance characteristics and thresholds in view of the teachings of Tobias, as doing so would give the added advantage of including fan control to help manage heat dissipation in the system in addition to the processor utilization increasing and decreasing (column 2, lines 15-25).

As to claim 22, Maitra discloses the computer program product wherein said is program instructions further comprise program instructions for: reading values ("accessing" information which necessitates reading) of a plurality of performance counters (Maitra discloses the clock scheduling unit collecting information from a task scheduler unit which prioritizes applications dependent on the amount of time used by the process which, as is known the art, necessitates performance counters to calculate usage; column 8, lines 55-61) during one or more previous execution slices (time quantum) of said next process (column 2, lines 49-67); and estimating ("prioritizing") said associated level of energy usage ("determines the amount of CPU time each

application receives") in conformity with said values of said plurality of performance counters (column 8, line 45 thru column 9, line 4).

As to claim 23, Maitra discloses the computer program product wherein said program instructions further comprise program instructions for: measuring ("retrieves information") actual energy usage of said processing system ("computing requirement") during one or more previous execution slices of said next process ("next quantum") (column 8, lines 47-64); and estimating ("determining") said associated level of energy usage in conformity with said measured energy usage (column 8, lines 47-64).

As to claim 24, Maitra discloses the computer program product wherein said program instructions further comprise program instructions for: second determining ("determines the applications run" via switch detection unit [210] found in clock scheduling unit [120 or 200]) a resource usage of said next process (column 5, lines 10-13 and column 5, lines 31-40 and column 5, line 54 thru column 6, line 14); and estimating ("determines the computing requirement" via application characterization unit [220]) said associated level of energy usage in conformity with said resource usage (column 6, lines 1-14).

As to claim 25, Maitra discloses the computer program product wherein said program instructions further comprise program instructions (column 5, lines 63-67) for receiving from an application owning said next process an indication of said resource usage (column 6, lines 4-14), and wherein said determining determines said resource usage ("computing requirements") in conformity with said received indication (column 6, lines 1-14).

As to claim 26, Tobias teaches the computer program product wherein said program instructions for second determining further comprise program instructions for observing prior allocation of resources to said next process (column 4, lines 52-67 and column 2, lines 15-25).

As to claim 27, Tobias teaches the computer program product wherein said program instructions further comprise program instructions for: issuing a pragmatic warning fault ("bit being sent") indicating that a system energy usage above a system energy threshold (column 1, lines 39-42); and receiving ("predicting" heat based on CPU performance which necessitates receiving) said pragmatic warning fault ("performance indicators") at an application associated with said next process, and in response to said receiving, reducing a resource usage within said application, whereby a energy usage of said next process is reduced (column 2, lines 26-42).

As to claim 28, Tobias teaches the computer program product wherein said program instructions further comprise program instructions for: issuing ("signal indicative of the temperature of system [100] is received and processed") a critical pragmatic fault indicating ("failsafe signal") that said system energy usage has not been reduced below said system energy threshold (column 4, lines 25-36); and receiving ("control transitions" which necessitates receiving) said critical pragmatic fault at said scheduler (control daemon), and wherein said selectively scheduling is performed in response to said receipt of said critical pragmatic fault by said scheduler (Tobias discloses a flowchart [figure 2] which reveals the steps needed in decision making of altering the fan speed wherein said flow returns to step 210 repetitively wherein flow could flow to normal alteration to step 240 or to a critical response to 230; column 4, lines 25-36).

As to claim 29, Maitra discloses the computer program product wherein said program instructions for selectively scheduling insert idle slices ("device may be turned off" or "asserts and de-asserts an internal clock divider mechanism in the processor") into an execution queue ("list of applications that need to be run"), whereby said energy usage level is reduced (Maitra discloses time slices places into a list of applications to be run wherein said clock to functional units within the processor can be de-asserted if not needed which therefore necessitates inserting idle slices [periods of inactivity]; column 1, line 63 thru column 2, line 1 and column 4, lines 35-55 and column 5, lines 33-40).

As to claim 30, Maitra discloses the computer program product wherein said program instructions for selectively scheduling schedule a second process having a lower level of energy usage than said next process in preference over said next process (Maitra discloses a priority list of applications being implemented wherein applications are run dependent on the size of the quantum such that internally defined priorities can decide which applications run next dependent on their high or low energy usage; column 4, lines 44-55).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

James Sugent
Patent Examiner, Art Unit 2116
March 29, 2006